Bandwidth Improvement using Pulse Compression within an Electro-optic System for High Bit Rate Telecommunications

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Abstract **– The dispersive and attenuation properties of multilayer telecommunication line cards are discussed as part of 10 Gbit/s OC192 telecommunications systems. A number of different methodologies are described to compensate for dispersion, attenuation and general signal distortion within high bit rate electro-optic telecommunications systems. This work will report the use of pulse compression techniques to reduce distortion within conventional multilayer circuit boards. This is achieved using a non-linear transmission line which uses the non-linear capacitance-voltage (CV) characteristic of hyper-abrupt Schottky diodes to provide the non-linear function. The development of the Schottky diode based on silicon technology is reported and is explained. The special circuit topology chosen for this circuit enables both rising and falling edge compression. Using this approach the higher harmonic content of fast pulses is reconstructed and signal dispersion in the transmission line is compensated.**

1. INTRODUCTION

The need to transmit gigabit data streams within optical networking equipment, such as routers and switches, is driving the need for increasing the aggregate bandwidth through the copper medium of the interface card. Developments in fiber optic cable technology and in optical signal regeneration enables digital data transmission for long distances at high bit rates without any significant distortion. Inside the backplane, however, the medium of transmission is conventional copper printed circuit board (PCB) traces with distances of up to 50 cm within a multilayer interconnect environment.

These transmission mediums have attenuation and delay distortion (dispersion) which is extremely high compared to optical fiber. The small resistances and inductances of the interconnects and the vias inside the telecommunications line cards and the backplane function as low pass filters limiting the high frequency components of the digital pulses. All of these factors together cause significant distortion within digital pulses and increase the rise and the fall time of the signal edges (causing the signal pulse to take on a Gaussian shape). As a result, the inter-symbol interference (ISI) and the bit error rate (BER) are increased significantly. The high ISI and BER limit the transmission frequency in the backplane card system and considerably reduce the optimum system bandwidth.

Currently, active research is ongoing to reduce the ISI due to these factors in the backplane system. The aim of this work is to transmit 10 Gbit/s of data over a single trace of a multilayer telecommunications line card whilst maintaining a useable eye diagram for long signal traces.

Some recent research has been devoted to the design of equalizer circuits on silicon that removes this signal distortion by using multilevel logic approaches. These circuits show some improvement in ISI reduction and in eye diagram opening, but the percentage of error is still high.

Another solution to this problem is realized using pulse compression circuits, where the lost or attenuated harmonics are regenerated by using a form of non-linear wave propagation. This phenomenon is observed in the non-linear transmission line (NLTL) as well as in the fibre optics line and is the method investigated in this work.

The NLTL is a high impedance transmission line loaded by reverse biased Schottky varactor diodes. The non-linear CV characteristics of the Schottky diode are the source of the non-linearity element that is responsible for the harmonic regeneration and pulse compression. A schematic diagram of the NLTL is shown in Fig.1.
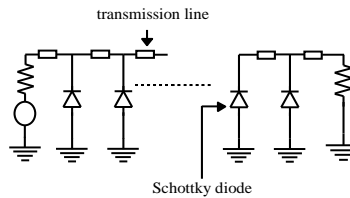

Figure 1 Schematic diagram of the NLTL.

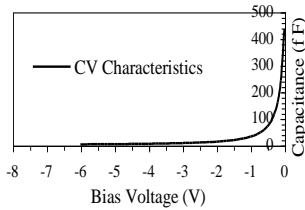Typical CV characteristics of the diode are shown in Fig.2.

Figure 2 Typical CV characteristics of the Schottky diode.

NLTL circuits with very sharp fall or rise time have been realized on GaAs circuits [1]-[5]. In this paper silicon NLTLs will be designed for this purpose. Although their performance is less than III-V compound semiconductors, they do have the advantage of much cheaper processing for the High Resistivity Silicon (HRS) substrate and the possibility to use more diode stages due to the availability of more chip area.

The silicon Schottky diode has lower carrier mobility compared with GaAs or Indium Phosphide [6]. This reduces the silicon Schottky diode performance especially for high frequency applications. Another disadvantage with the silicon Schottky diode is the inheritance of large series resistance. This decreases the cutoff frequency of the diode and increases the losses in the NLTL. Hence there is a specific requirement to design novel silicon Schottky diode structures with less series resistance and small dimensions to achieve the high cutoff frequencies required.

2. BACKGROUND THEORY

In this work the NLTL is designed as a schock wave generator, where the signal at the output of the NLTL has a fall time which is eight times faster than the input signal at Full Wave Half Maximum (FWHM). The equivalent circuit of the NLTL is given in Fig.3.
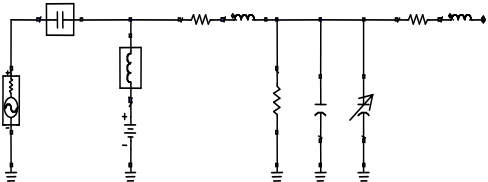

Figure 3 Equivalent circuit of the NLTL.

Theory of operation of the NLTL can be understood from the speed of propagation on the NLTL where the speed of propagation is given by (assuming lossless NLTL operation) [7].

$$v = \frac{1}{\sqrt{L(C + C_d(V)}}\qquad(1)$$

Where v is the speed of propagation, L, C are the inductance and the capacitance per section of the hosting line and $C_d(V)$ is the junction capacitance of the Schottky diode as a function of the applied voltage.

From equation (1) the higher amplitude voltage signals travels faster than the lower amplitude ones. This difference in the propagation speed shortens the fall time of the propagating signal at the expense of expanding the rising time to the same signal. The opposite operation is noticed if the Schottky diode is reversed and the bias voltage is also reserved. After a sufficient number of sections a shock wave is generated at the output of the NLTL. Increasing the number of sections will increase the compression ratio of either the fall or the rise time of the signal as it propagates down the NLTL. After a sufficient number of sections, the compression generated by the NLTL is balanced by the dispersion generated in the NLTL itself. At this stage, increasing the number of sections of the NLTL will increase the losses without any further increase of the compression ratio.

A single NLTL is not very helpful in reducing the ISI because of the trailing edge expansion problem. In this paper a novel circuit is proposed using two NLTLs. One of them processes the rising edge of the input waveform and the other one processes the falling edge of the digital pulse. A square shaped pulse is generated at the output, if the output of two similar NLTLs is combined using a Wilkinson power combiner circuitry. The schematic diagram of this proposed circuit is explained in Fig.4.
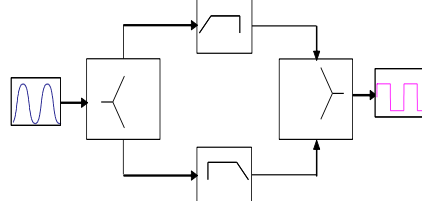

Figure 4 Pulse compression circuit using 2 NLTLs and Wilkinson power combiner circuitry.

It is expected that this circuit will compensate for the dispersion due the long traces of the PCB. It is also expected that the lost harmonics due to the Low Pass Filter (LPF) characteristics of the interconnects on the daughter cards are regenerated again to restore the original shape of the signal. The attenuation due the daughter card in the backplane system and due to the pulse compression circuit are compensated by using long tailed pair DC–amplifier

3. FABRICATION PROCESS

Hyper abrupt Schottky diodes are used in the design of the NLTL because of their highly non-linear CV characteristics. Although the nonlinearity of the hyperabrupt Schottky diode is less than that of the delta-

doped Schottky diode [8], the cut off frequency of the hyper abrupt diode is higher than the delta-doped diode because it does have smaller series resistance. A cross sectional area of the proposed diode is given in Fig. 5.
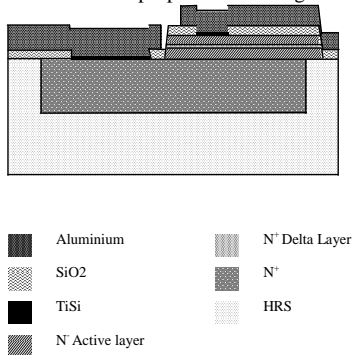

▨	Aluminium	▦	N⁺ Delta Layer
▨	SiO2	▩	N⁺
■	TiSi	▨	HRS
▨	N⁻ Active layer		

Figure 5 Cross section of the hyper abrupt silicon Schottky diode with n⁺ layer for reduced series resistance.

The diode is fabricated using the ion implantation and the ion splitting technique [9].In this way a very conductive n⁺ region is added to the diode structure without altering the properties of the ion implanted waver. The purpose of adding this heavily doped region is to reduce the Schottky diode series resistance.

In this work the NLTL is integrated on MMIC circuit. Several diodes with different sizes are proposed on the same chip for the purpose of testing. The wafer support diodes suitable for both DC and microwave testing are. It also include different NLTLs as shown in Fig.6.
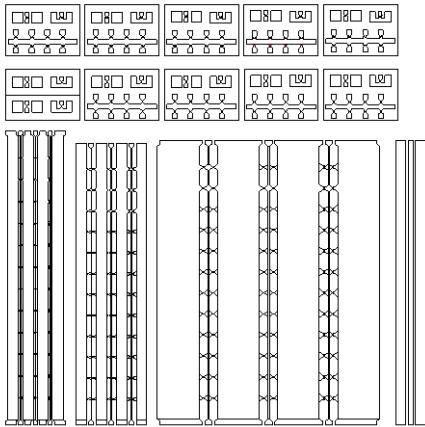

Fig. 6.   Top layer mask for diode test structures and 12 sections NLTL

pulse compression circuits.

4. SIMULATION RESULTS

Prior to fabrication, extensive simulations are done on the diode to optimize the CV characteristics and the series resistance using Silvaco™. The extracted CV characteristics of the Schottky diode are curve fitted to a sigmoid function for the use in ADS™. The input and the output signals are simulated using the Harmonic Balance (HB) simulation technique available in the ADS™. The time domain of the input and the output voltages are shown in Fig.7.

The frequency contents of the output signal are shown in Fig.7 (b). Fig.7 (b) shows that the output signal contains the even and the odd harmonics. The presence of the even harmonics in Fig. 7(b) explains why the NLTL expands the rise or the fall time of the output wave. Understanding of this result is well-known from the Fourier analysis of the square pulse. Fourier analysis of the square pulse shows that it contains an infinite number of odd harmonics and it does not have any of the even harmonics.
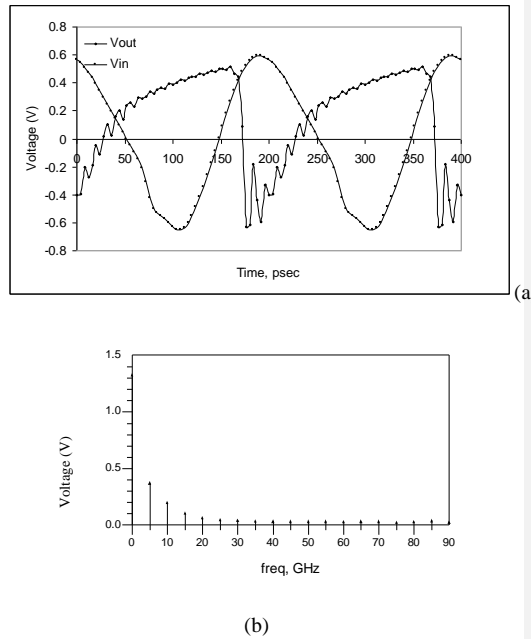

(a)

(b)

Figure 7 (a) Input and output signal on the NLTL in the time domain. (b) Frequency contents of the signal at the NLTL output.

The impact of the pulse compression circuit on the eye diagram improvement of the system is simulated using the co-sim feature within the ADS™. Using this facility, ADS™ can simulate a complete system and provide an estimate for what is happening inside that entire system.

Plotting the eye diagram of the system without using the Pulse compression circuit shows that the eye opening is completely closed. Simulation shows that an improvement of the eye diagram opening is observed when the pulse compression circuit is added to the system. The eye diagram of the system before and after the use of the pulse compression circuit is given in Fig. 8
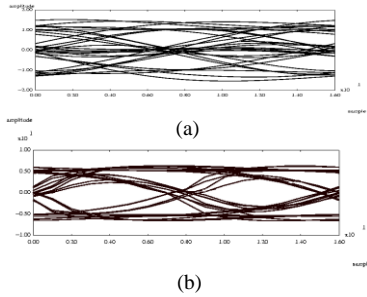

(a)

(b)

Figure 8 (a) Eye diagram of the system without the pulse compression circuit. (b) Eye diagram of the system with the pulse compression circuit.

5. MEASUREMENTS SETUP

…..Two types of measurement setups are required to study the performance of a single NLTL circuit; small and large signal measurements. The Agilent 8510B vector network analyzer (VNA) is used to perform small signal measurements. These measurements are used to extract the equivalent circuit of the Schottky diode using variable bias under small signal excitation. The measurement setup [10]; Fig.9 is composed of the VNA, synthesized sweeper, S-parameter test set and the device under test. In this case the device under test is the Schottky diode.
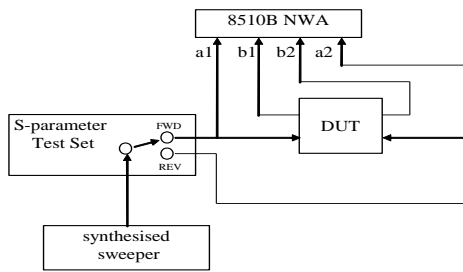

Figure 9 Small signal measurement setup system.

Before starting the measurement the system must be calibrated to account for the systematic errors. These errors are generated by the delays, losses and mismatches in the cables, the probe station and various circuitry of the measurement system. The Thru-Line-Reflect (TRL) calibration method is used to account for these errors and give reliable measurements.

The microwave transition analyzer (MTA) is used to measure the input and the output voltage waveforms either in the time domain or frequency domain under large signal conditions as would be the case in the NLTL. The measurement
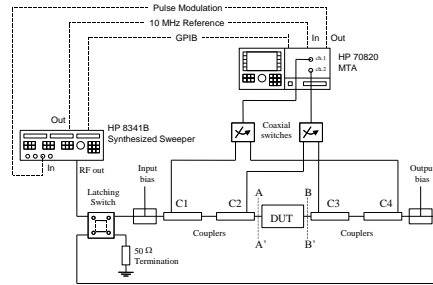

Figure 10 the large signal measurement system.

setup [11]; Fig.10; is composed of a synthesized sweeper to generate the input test signal. The input and output Bias Tees are used apply the bias voltage to the device under test (DUT) and the directional couplers at the input and output are used to measure the incident and reflected waves not only at the fundamental frequency of the periodic pulse but also at related harmonic frequencies up to 40 GHz. Due to the vector nature of the system both fundamental and harmonic magnitude and phase can be accurately measured up to 40 GHz permitting the current and voltage waveforms to be measured at the input and output of the fabricated NLTL. The switches are used to direct the signals measured by the MTA for either forward or reverse measurement.

This non-linear large signal measurement system is used to measure the input and the output voltages on the designed NLTL. The circuit of the NLTL in this case is composed of eight sections. Measured and simulated data shows a very strong agreement as shown in Fig.11
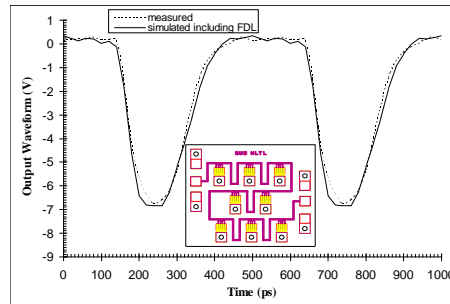

Figure 11 Measured and simulated output wave forms on a NLTL designed at Queens University

6. CONCLUSION

The use of the NLTL circuitry for pulse compression (shock wave generator) shows some improvement in the opening of the system's eye diagram. This circuit have promising features in increasing the bandwidth on conventional copper transmission systems, where 10 Gbit/s can be transmitted over single trace.

ACKNOWLEDGEMENT

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